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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
DINH, PAUL

ART UNIT	PAPER NUMBER
2825	

John W. Carpenter
CROSBY, HEAFEY, ROACH & MAY
P.O. Box 7936
San Francisco, CA 94120-7936

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/919,740	ELASSAAD ET AL.	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 16-35* is/are pending in the application.

4a) Of the above claim(s) *20-26* is/are withdrawn from consideration.

5)☒ Claim(s) *27-30* is/are allowed.

6)☒ Claim(s) *1-5,7,9 and 13-19* is/are rejected.

7)☒ Claim(s) *6,8,10-12 and 31-35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Note: claims 10-12 duplicate claims 31, 34-35, see claim objections in detailed office Action PD

Application Papers

9)☐ The specification is objected to by the Examiner. claims 10-12 should be cancelled.

10)☒ The drawing(s) filed on *16 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Paul Dinh

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

- This FINAL OFFICE ACTION is a response to the amendment+ remarks filed on 6/16/05.
- The remarks regarding the prior art of record Van Ginneken, Le, and Boyle are persuasive; therefore, the rejections based on Van Ginneken, Le, and Boyle have been withdrawn.
- The remarks regarding the prior art of record Alpert are not persuasive; therefore, the rejections based on Alpert are retained; see the following details.

Pending Claims

Claims 1-14, and 16-19 = original/amended.

Claims 20-26 = withdrawn (Applicant is advised to cancel the withdrawn claim in response to this FINAL OFFICE ACTION)

Claims 27-35 = new.

Claim Objections

1. Claims 10-12 are objected to under 37 CFR 1.75 as being substantial duplicates of new claims 31, 34-35. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

The following compares claim duplication:

Claim 10 duplicates new claim 31.

Claim 11 duplicates new claim 34.

Claim 12 duplicates new claim 35.

Note that:

a. Original-dependent claim 10 (claim 10 directly/indirectly depending on and including the limitations of claim 9 and claim 1), was an allowable subject matter in the last office action, and now being a substantial duplicate of new independent claim 31; **and**

b. Applicant should cancel claims 10-12 to overcome claim duplicates.

2. Claim 31 is objected to because on line 16, a colon (:) should be used after the word "comprises", not a comma (,) and the limitations after line 16 should be separated by semicolons (;), not commas (,). **Correction is required.**

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis For the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 7, 9; 13-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Alpert et al (US Patent Application No. 2002/0184607)

(Claims 1, 16-19)

Preparing a physical hierarchy of the circuit design with placed macros (fig 1, 4-5);

Performing global routing on the physical hierarchy (para 0006, 0009, 0012. 0035, 0047-0048, 0057);

Determining a number of buffers to be inserted on each edge of nets of the global routing for boosting timing performance of the nets (para 0007, 0048);

Calculating a position for each buffer (abstract, summary, para 0042, claim 1); and

Inserting a buffer configured to boost timing performance at each calculated position (para 0005, 0007, 0043).

(Claims 2-3) wherein said buffers are inverters/repeaters (para 0004, 0036, 0047).

(Claims 4-5) identifying a set at least one edge in said nets for inserting buffers; and determining an optimal number of buffers to be inserted on each edge (fig 3-12), calculating, for each edge, the optimal number of buffers based on an optimal timing for the edge, a delay of the edge, and an impedance of the edge (fig 3-12).

(Claims 7, 9) determining a uniform load distribution for all branches connected to the edge; and adjusting for a delay introduced by the inserted buffers (para 0071, 0073), uniformly distributing a capacitance of each branch of the nets at a corresponding branch point; determining

a load at each branch point; and checking if a buffer inserted at each branch point is capable of handling the load determined for that branch point (para 0071, 0073).

(Claims 13-14) said method is embodied in a set of computer instructions stored on a computer readable media; said computer instructions, when loaded into computer, cause the computer to perform the steps of said method (fig 2); wherein said computer instructions are compiled computer instructions stored as an executable program on said computer readable media (fig 2)

Response to Applicant Remarks

The applicant states that Alpert does not teach or suggest "**determining a number of buffers to be inserted on each edge of nets of the global routing for boosting timing performance of the nets**".

Here are examiner answers:

Alpert does teach "**determining a number of buffers to be inserted on each edge of nets of the global routing**" in paragraph 0048.

Paragraph 0048 "A tiling is represented by a graph G (V,E) where V is the set of tiles and edge e.sub.u,v is in E if u and v are neighboring tiles. Given a tile v, let B(v) be the number of buffer sites within the tile. Let N=[n.sub.1, n.sub.2, . . . , n.sub.m] be the set of global nets and let W(e.sub.u,v) be the maximum permissible number of wires that can cross between u and v without causing overflow. If b(v) denotes the number of buffers assigned to v, the buffer congestion for v is given by b(v)/B(v). Similarly, given a global routing of N, if w (e.sub.u, v) denotes the number of wires which cross between tiles u and v, the wire congestion for edge e.sub.u, v is given by w (e.sub.u, v)/W (e.sub.u, v)."

The limitation "**for boosting timing performance of the nets**" is inherent with buffer insertion. Buffer insertion inherently boosts timing performance because buffer insertion provides: control/improvement/ fix/ reduction/limit/optimization/correction of: delay, capacitance/impedance/parasitic, timing constraint/violation, length constraint, timing reflection, signal skew/slew, and wire length of nets; these are the attributes that affect timing performance of nets.

For applicant information, Alpert also teaches the inherent feature of boosting timing performance of the nets with buffer insertion, i.e.,

Para 0004 "Buffer insertion has become a critical step in deep submicron design as interconnect now plays a dominating role in determining system performance. The insertion of buffers and inverters on signal nets can provide several advantages, including reducing interconnect delay, restraining noise, improving the slew rate, and fixing electrical violations"

Para 0006-0007 "to manage the large number of buffers and also achieve high performance on the critical global nets, buffers must be planned for early in the design" "buffer can be inserted for a particular net such that the net's timing constraint is satisfied."

Para 0043 "timing constraints are generally not available since macro block designs are incomplete and global routing and extraction have not been performed. Potentially crude timing analysis could be performed, but the results are often grossly pessimistic because interconnect synthesis has not taken place. At this stage, one needs to globally insert buffers while tracking wire congestion"

Para 0047 "rule of thumb was also used for buffer planning by Dragan et al., "Provably Good Global Buffering Using an Available Buffer Block Plan", to appear in IEEE/ACM Intl. Conf. on Computer-Aided Design, pp. 104-109, 2000. They note that for a high-end microprocessor design in 0.25 micron (.mu.m) CMOS technology, repeaters are required at intervals of at most 4500. mu.m. Such a rule is necessary to ensure that the slew rate is sufficiently sharp"

Para 0063 "Once a low congestion routing exists, the next step assigns buffer sites to each net. This assignment is performed iteratively in order of net delay, starting with the net with highest delay"

Allowable Subject Matter

Claims 6 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 27-30 are allowed

Claims 31-35 would be allowable if their above-mentioned duplicates (claims 10-12) are canceled.

Reasons for Allowance

Claims 6, 8, 31-35 would be allowable and claims 27-30 are allowed because the prior art does not teach or suggest the limitations:

The step of calculating the optimal number of buffers as recited in claim 6;

The step of determining a uniform load distribution comprises calculating a stage delay for each branch as recited in claim 8 and claim 29;

The step of calculating the optimal number of buffers comprises calculating a capacitance Cx for each branch as recited in claim 27; and

The steps of determining a number of buffers and calculating a position of each buffer as recited in claim 31.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Dinh
Patent Examiner